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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,662	02/20/2004	Peter C. Salmon	34091/AJT	7233

7590 11/28/2006

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EXAMINER	
CLARK, SHEILA V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,662	SALMON, PETER C.	
	Examiner	Art Unit	
	S. V. Clark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *1-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim 8 is objected to as being improperly dependent upon multiply dependent claim 6, whereby a multiply dependent claims can not depend on another multiply dependent claim.

Claims 6, 19, 20, 24, 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 6, there is only a reference to "chips" where claim 1 may also include a single "chip".

In claims 19-20, it is unclear what is meant by the term "supergroup" Since the term " supergroup" may have many varying meanings said terms

should be defined in the claims.

In claim 24, there is no "imprintable material" recited in claim 17 nor any of the device claims.

In claims 25, there is no " thermoplastic material" recited in claims 17 nor any of the subsequent device claims

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 10, 11, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forehand et al

Forehand et al. teaches in for example figure 3, an electrically conductive substrate 220 having conductive feedthroughs 221-227 in said conductive substrate, a multi-layer interconnection circuit 203 having conductive traces (not shown but said traces are taught in col. 2, lines 59-63) fabricated on said conductive substrate; one or more integrated circuit chips 202 having bumps 205 that attach to selected traces of said interconnection circuits; and, wherein selected of said feedthroughs are shown connect with selected traces of said interconnection circuits.

With regard to claim 3, as Forehand et al has identified component 202 as an "integrated circuit chip" it would have been obvious to one having ordinary skill in this art that that said chip may be a radio frequency transceiver due to the broad use of "integrated circuit chip" would be suggestive that the teachings in the Forehand reference would be applicable to any conventional chip well known in this art.

As the claim fails to be specific relative to the word "connect" where in the claims it recites that "feedthroughs connect with ...traces" whereby connect can be mechanical or electrical said "connect" has been taken as an electrical connection whereby the traces that are taught but not shown to be on the upper surface of the interconnection circuit are deemed to be obviously electrically connected to the feedthroughs on substrate 220 by way of vias 207 and bumps 219.

With regard to claim 4, it would have been obvious to one having ordinary skill in this art that said attachment of said bumps of Forehand would include a well filled with solder interposed between each of said bumps and each of said traces because the bumps 205 of Forehand are identified as solder bumps would obviously suggest solder attachment between the bumps and the traces.

With regard to claims 10-12, the multilayerd circuit 203 is shown to possess alternative layer of patterned conductive material and dielectric material as recited in claim 10. Col. 3, line 47 identifies said dielectric layers as being "insulating", which suggests use of conventional materials including thermoplastic materials well known in the art including the use of liquid crystal polymer.

Claims 2, 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa.

Kurokawa teaches in figure 6 an electronic module comprising an electrically conductive substrate 47, a multi-layer interconnection 41b circuit having conductive traces (not labeled but shown) fabricated on said conductive substrate via wires 46; one or more integrated circuit chips 42 having bumps 43 that attach to selected traces of said interconnection circuits; and, one or more cable wire 46 having bumps that attach to selected traces of said interconnection circuit.

Though Kurokawa fails to specifically label wires 46 as cables he characterizes said wires broadly as " flexible wiring circuit members" formed of insulator film and copper conductors which have the same characteristics as "cable". It would have been therefore obvious to one having ordinary skill in this art that the cable like characteristics of wiring 46 would render said wiring as " cable" especially since the claims fail to render any specific descriptive characteristics to further characterize the word " cable" recited in the claims.

With regard to claims 3, Kurokawa has identified component chip 42 as a "semiconductor device chip" it would have been obvious to one having ordinary skill in

this art that that said chip may be a radio frequency transceiver due to the broad use of "semiconductor device chip" would be suggestive that the teachings in the Kurokawa reference would be applicable to any conventional chip well known in this art.

Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forehand et al

Forehand et al. teaches in for example figure 3, an electrically conductive substrate 220, a multi-layer interconnection circuit 203 having conductive traces (not shown but said traces are taught in col. 2, lines 59-63) fabricated on said conductive substrate connected to pads (not shown) on the upper surface of said interconnection circuit. One or more integrated circuit chip modules 202 having bumps 205 attached to selected pads.

As flip chip bumps are inherently connected to the input/output structures of a chip and to associated substrate input/output substrate pads it would have been considered obvious to one having ordinary skill in this art that the pads of Forehand et al are input/out put pads for the reasons just expressed. Further input/output pads are implied in the input/output discussion in col.3, lines 20-21.

Claims 5,7, 8, 9, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa.

Kurokawa teaches in for example figure 6, an electrically conductive substrate 47,a multi-layer interconnection circuit 1b having conductive traces (not labeled but shown) fabricated on said conductive substrate via wiring 46 and connected to pads (not shown) on the upper surface of said interconnection circuit. One or more integrated circuit chip modules 42 having bumps 43 attached to selected pads.

As flip chip bumps are inherently connected to the input/output structures of a chip and to associated substrate input/output substrate pads it would have been considered obvious to one having ordinary skill in this art that the pads of Kurokawa are input/out put pads for the reasons just expressed.

With regard to claims 7, 8, 9, figures 4 and 5 of Kurokawa teach use of a top conductive plate 45 (i.e. copper) formed on the back of modules 42.

With regard to claim 14, said top plate may contain a cooling chamber 48 where cooling fluid may circulate.

Claims 1, 3, 4, 6, 10, 11, 12, 13, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Honda.

Honda teaches in for example in the various views of figure 3, an electrically conductive substrate 11 having conductive feedthroughs 13 in said conductive substrate, a multi-layer interconnection circuit 9 having conductive traces 6 fabricated on said conductive substrate; an integrated circuit chip 14 having bumps 15 attached to selected traces of said interconnection circuits wherein selected ones of said feedthroughs are shown connect with selected traces of said interconnection circuits.

Though substrate 11 is identified as an insulating substrate said substrate one of ordinary skill in this art would obviously know that since said substrate contains conductive vias said substrate is therefore an electrically conductive substrate comprising an insulating layers and conductive vias and therefore obviously conductive.

With regard to claim 3, as Honda has identified component 14 as a "conventional flip chip type semiconductor device" (paragraph 004), it would have been obvious to one having ordinary skill in this art that that said chip may be a radio

frequency transceiver due to admission by Honda of the chip of his invention as "conventional" suggesting that the teachings in the Honda would be applicable to any conventional chip well known in this art.

With regard to claim 4, it would have been obvious to one having ordinary skill in this art that said attachment of said bumps of Honda would include a well filled with solder interposed between each of said bumps and each of said traces because the bumps 15 of Honda are identified as solder bumps would obviously suggest solder attachment between the bumps and the traces.

With regard to claims 6 and 9, figures 4 and 5 of Honda teach use of a top conductive plate 19 (i.e. copper) formed on the back of chip 14.

With regard to claims 10-12, the multi-layered circuit 9 is shown to possess alternative layer of patterned conductive material and dielectric material as recited in claim 10. Paragraph (0055) identifies dielectric layers 3 as being formed of resin and therefore formed of a thermoplastic material. As well known to one having ordinary skill in this art that the use of conventional materials such as thermoplastic materials would further suggest that it would also be well known in the art that these materials would include the use of conventional polymer resins such as liquid crystal polymer.

With regard to claims 13, traces 6 are taught to be formed of copper in paragraph (0058).

With regard to claim 15, said bumps may be formed of gold (see paragraph (0068).

With regard to claim 16 it would have been obvious to one having ordinary skill in this art that said attachment of said bumps of Honda would include a well filled with

solder interposed between each of said bumps and each of said traces which is provided in a layer on the top of said interconnection because the bumps 15 of Honda are identified as including solder which would obviously suggest solder attachment between the bumps and the traces.

Claims 17, 18, 21, 23, 26, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Honda.

Honda teaches in for example in the various views of figure 3, an electrically conductive substrate 11, a multi-layer interconnection circuit 9 formed thereon having conductive traces 2, 5, 6 terminating at pads 6 fabricated on said conductive substrate, a plurality of integrated circuit flip chips 14 (see plurality in figure 6G) having bumps 15 attached to selected traces of said interconnection circuits.

Further as the claim fails to define what is meant by "blade" the term has been taken to mean "an interconnect structure" in the broadly which Honda is deemed to teach.

Further as flip chip bumps are inherently connected to the input/output structures of a chip and to associated substrate input/output substrate pads it would have been considered obvious to one having ordinary skill in this art that the pads 6 of Honda are input/out put pads for the reasons just expressed.

It would have been obvious to one having ordinary skill in this art that said attachment of said bumps of Honda would include a well filled with solder interposed between each of said bumps and each of said traces which is provided in a layer on the top of said interconnection because the bumps 15 of Honda are identified as including

solder which would obviously suggest solder attachment between the bumps and the traces.

With regard to claim 18, as Honda has identified component 14 as a " conventional flip chip type semiconductor device" (paragraph 004), it would have been obvious to one having ordinary skill in this art that that said chips may include logic, memory, and communication functions due to admission by Honda of the chip of his invention as "conventional" suggesting that the teachings in the Honda would be applicable to typical chips formed in semiconductor devices which are well known in this art.

With regard to claims 21 and 23, figures 4 and 5 of Honda teach use of a top conductive plate 19 (i.e. copper) formed on the back of chip 14.

With regard to claim 26, traces 6 are taught to be formed of copper in paragraph (0058).

With regard to claim 27, said bumps may be formed of gold (see paragraph (0068).

Claims 17, 21, 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa.

Kurokawa teaches in for example figure 6, an electrically conductive substrate 47, a multi-layer interconnection circuit 41b formed thereon having conductive traces (not labeled but shown) terminating at pads (now labeled but shown) fabricated on said conductive substrate, a plurality of integrated circuit flip chips 42 having bumps 15 attached to selected traces of said interconnection circuits and said bumps would be inherently connected to pads that are connected to said traces.

Further as the claim fails to define what is meant by "blade" the term has been taken to mean "an interconnect structure" in the broadly which Kurokawa is deemed to teach.

Further as flip chip bumps are inherently connected to the input/output structures of a chip and to associated substrate input/output substrate pads it would have been considered obvious to one having ordinary skill in this art that the pads 6 of Kurokawa are input/out put pads for the reasons just expressed.

It would have been obvious to one having ordinary skill in this art that said attachment of said bumps of Kurokawa would include a well filled with solder interposed between each of said bumps and each of said traces which is provided in a layer on the top of said interconnection because the bumps 15 of Kurokawa are identified as including solder which would obviously suggest solder attachment between the bumps and the traces.

With regard to claims 21 and 23, figure 6 of Kurokawa teach use of a top conductive plate 45 (i.e. copper) formed on the back of chips 42.

With regard to claim 22, said top plate may contain a cooling chamber 48 where cooling fluid may circulate and said plate is connected to conducting substrate 47 and is deemed coextensive with said substrate which includes the blades.

Certain claims contain method of making characteristics (i.e. electroplated, replaced with) given no patentable weight in determining the patentability of the final device product.

Note that a Aproduct by process≅ claim is directed to the product per se, no matter how actually made, In re Hirao 190 USPQ 15 at 17(footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessman, 180 USPQ 324; In re Avery, 186 USPQ 161 and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a product by process≅ claims, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in a product by process claims or not.

Claims 1-27 are rejected.

The election of claims 1-27 without traverse in the communication filed March 29, 2005 is acknowledged.

PTO-892 cites references having multilayer substrates.

Any inquiry concerning this communication should be directed to S. V. Clark at telephone number (571) 272-1725.

S. V. Clark
Primary Examiner
Art Unit 2823

November 14, 2006

Notice of References Cited	Application/Control No. 10/783,662	Applicant(s)/Patent Under Reexamination SALMON, PETER C.	
	Examiner S. V. Clark	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0121689	09-2002	Honda, Hirokazu	257/700
*	B	US-5,239,448	08-1993	Perkins et al.	361/764
*	C	US-5,640,051	06-1997	Tomura et al.	257/778
*	D	US-6,784,554	08-2004	Kajiwara et al.	257/778
*	E	US-6,392,301	05-2002	Waizman et al.	257/774
*	F	US-5,281,151	01-1994	Arima et al.	439/68
*	G	US-5,291,064	03-1994	Kurokawa, Yasuhiro	257/714
*	H	US-5,847,936	12-1998	Forehand et al.	361/794
*	I	US-6,956,285	10-2005	Radu et al.	257/697
*	J	US-6,891,732	05-2005	Takano et al.	361/783
*	K	US-5,510,758	04-1996	Fujita et al.	333/247
*	L	US-5,635,767	06-1997	Wenzel et al.	257/778
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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